What is claimed is:

1. A data output buffer circuit in a semiconductor memory device, comprising:

driving means for receiving pull-up and pull-down control signals and driving a data output terminal with voltage levels corresponding to data read from a memory cell; and

controlling means for supplying the driving means with control signals to delay the first output of the read data for a designated delay time, and to cause the output of the driving means to retain high impedance state during the designated delay time.

2. The data output buffer circuit as recited in claim 1, wherein the controlling means delays the first output of the read data so as to meet the 'tLZ' specification, the data output time from an external reference clock.

3. The data output buffer circuit as recited in claim 2, wherein the control signal is generated by delaying a data out enable signal.

4. The data output buffer circuit as recited in claim 3, wherein the data out enable signal maintains a first logic value before a data read command is activated, and maintains a second logic value as much as burst length of the output data

while the data read command is activated.

5. The data output buffer circuit as recited in claim 4, wherein the data out enable signal maintains the first logic value while the output of the driving means needs the maintenance of high impedance state, and maintains the second logic value while the read dada is being outputted.

6. The data output buffer circuit as recited in claim 3, wherein the controlling means comprises:

a delaying part for generating the control signal by delaying the data out enable signal; and

a switching part for causing the two input terminals of the driving means to take either designated logic values setting high impedance state to the output in response to the control signal or the logic values of the pull-up and pull-down control signals.

7. The data output buffer circuit as recited in claim 6, wherein the delaying part includes at least 2 levels of a unit delaying part having an inverter chain structure.

8. The data output buffer circuit as recited in claim 7, wherein the controlling means adjusts the amount of delay by changing the number of levels of the unit delaying part.

9. The data output buffer circuit as recited in claim 6,

wherein the switching part comprises:

a first inverter for complementing the control signal; and

a switching transistor taking the signal as gate input, one side thereof connected to the ground voltage terminal, the other side thereof commonly connected to the two input terminals of the driving means.

10. A data output buffer circuit in a semiconductor memory device, comprising:

a latch means for holding pull-up and pull-down control signals corresponding to data read from a memory cell;

a data out driver for amplifying and outputting the output of the latch means; and

a controlling means for supplying the latch means with control signals to delay the first output of the read data for a designated delay time, and to cause the output of the data out driver to retain high impedance state during the designated delay time.

11. The data output buffer circuit as recited in claim 10, wherein the controlling means delays the first output of the read data so as to meet the 'tLZ' specification, the data output time from an external reference clock.

12. The data output buffer circuit as recited in claim 11, wherein the control signal is generated by delaying a data

out enable signal.

13. The data output buffer circuit as recited in claim 12, wherein the data out enable signal maintains a first logic value before a data read command, and maintains a second logic value as much as burst length of output data upon the data read command.

14. The data output buffer circuit as recited in claim 13, wherein the data out enable signal maintains the first logic value while the output of the data out driver needs the maintenance of high impedance state, and maintains the second logic value while the read dada is being outputted.

15. The data output buffer circuit as recited in claim 12, whereinthe controlling means comprises:

a delaying part for generating the control signal by delaying the data out enable signal; and

a switching part for causing the two input terminals of the latch means to take either designated logic values setting high impedance state to the output in response to the control signal or the logic values of the pull-up and pull-down control signals.

16. The data output buffer circuit as recited in claim 15, wherein the delaying part comprises at least 2 levels of a unit delaying part having an inverter chain structure.

17. The data output buffer circuit as recited in claim 16, wherein the controlling means adjusts the amount of delay by changing the number of levels of the unit delaying part.

18. The data output buffer circuit as recited in claim 15, wherein the switching part comprises:

a first inverter for complementing the control signal; and

a switching transistor taking the signal as gate input, one side thereof connected to the ground voltage terminal, the other side thereof commonly connected to the two input terminals of the latch means.

19. The data output buffer circuit as recited in claim 10, further comprising:

a second inverter for complementing one of the two output signals of the latch means; and

a data out pre-driver taking as inputs both a complemented and non-complemented outputs from the latch means, and for driving the data out driver.

20. The data output buffer circuit as recited in claim 19, wherein the latch means comprises:

a first latch part, between one of the two input terminals and the second inverter, composed of two inverters cross-coupled together in a manner where the output of one is connected to the input of the other; and

a second latch part, between the other one of the two input terminals and the data out pre-driver, composed of two inverters cross-coupled together in a manner where the output of one is connected to the input of the other.